CLAIMS

1. A system comprising:

an SRAM memory device;

a clock; and

a digital signal processor coupled to the memory device and the clock, the digital signal processor including

a first stage having a plurality of absolute difference determinators to calculate the absolute difference of a plurality of data sets;

a second stage to combine the absolute differences of the plurality of data sets into at least two intermediate values for two different sum of absolute differences calculations wherein the second stage is provided by reconfiguring a multiplier; and

a third stage including at least two accumulators to accumulate each of the intermediate values to determine two sum of absolute differences values from the plurality of data sets in parallel.

2. The system of Claim 1, wherein each absolute difference determinator includes an arithmetic logic unit and a multiplexer.

3. The system of Claim 1, wherein the second stage includes at least one arithmetic logic unit.

4. The system of Claim 3, wherein the second stage provides at least two adder trees.

5. The system of Claim 1, wherein the third stage includes two accumulators to maintain a running total of the absolute differences from the first stage for each sum of absolute differences calculations.

6. The system of Claim 1, further comprising:

two adder trees, each of the adder trees operative to combine at least a portion of the plurality of absolute differences into a sum of absolute differences.

7. The system of Claim 6, wherein at least a portion of each of the adder trees is formed from a reconfigured multiplier.

8. The system of Claim 1, wherein the plurality of data sets represents a pixel of video information.

9. The system of Claim 8, wherein each pixel of video information from each of the plurality of data segments is combined to form an image.

10. The system of Claim 1, wherein the digital signal processor is used within a video display.